CLAIMS

1. A ball grid array mounted circuit comprising;

a stress relief substrate having a top surface and a bottom surface;

spaced conductive vias extending between the top surface and said bottom surface;

connection pads at said top surface with each connection pad capturing at least one of said vias;

connection pads at said bottom surface in registration with said connection pads at said top surface;

an electronic component having a first thermal coefficient of expansion (TCE) and having connection pads spaced to align with said connection pads at said top surface;

first solder connections formed from solder balls between said connection pads at said top surface and said component connection pads;

a printed circuit board (PCB) having a second TCE and having connection pads aligned with said connection pads at said bottom surface;

second solder connections formed from solder balls between said connection pads at said bottom surface and said PCB connection pads, wherein said first solder connections and said second solder connections are shaped to absorb at least a portion of the stress due to differences between said first TCE and said second TCE.

2. Ball grid array mounted circuit of claim 1 wherein said stress relief substrate comprises a flexible polyimide like material having a thickness in the range of about 2 to 5 mils.

3. Ball grid array mounted circuit of claim 1 wherein said electronic component connection pads have a size substantially larger than a size of said connection pads at said top surface and said first solder connections have a substantially smaller cross section at said pads at said top surface than at said component connection pads which acts to absorb at least a portion of the stress due to differences between said first TCE and said second TCE.

4. Ball grid array mounted circuit of claim 1 wherein said PCB connection pads have a size substantially larger than a size of said connection pads at said bottom surface and said second solder connections have a substantially smaller cross section at said pads at said bottom surface than at said PCB connection pads which acts to absorb at least a portion of the stress due to differences between said first TCE and said second TCE.

5. Ball grid array mounted circuit of claim 2 wherein said connection pads at said top surface capture a plurality of said conductive vias.

6. Ball grid array mounted circuit of claim 2 wherein said conductive vias have a diameter in the range of 1 to 5 mils and a pitch in the range of 2 to 10 mils.

7. Ball grid array mounted circuit of claim 2 wherein said connection pads at said top surface and said connection pads at said bottom surface have a diameter in the range of about 20 to 30 mils.

8. Ball grid array mounted circuit of claim 2 wherein said electronic component is a ceramic package having a TCE of about 7 ppm/degree C and said PCB has a TCE in the range of about 12-25 ppm/degree C

9. Ball grid array mounted circuit of claim 2 wherein said electronic component is a chip scale package and said conductive vias have a pitch in the range of about 10 to 40 mils.

10. Ball grid array mounted circuit of claim 2 wherein said electronic component is a ruggedized die having an array of pads suitable for mounting to a PCB.

11. Ball grid array mounted circuit of claim 2 wherein said conductive vias are located in said flexible substrate only at said connection pads.

12. A ball grid array mounted circuit comprising;

a stress relief substrate having a top surface and a bottom surface;

spaced conductive vias extending between the top surface and said bottom surface;

connection pads at said top surface with each connection pad capturing at least one of said vias;

connection pads at said bottom surface in registration with said connection pads at said top surface;

an electronic component having a first thermal coefficient of expansion (TCE) and having connection pads spaced to align with said connection pads at said top surface, said electronic component connection pads being of a larger size than said connection pads at said top surface;

solder connections formed from solder balls between said connection pads at said top surface and said component connection pads, with said larger size pads causing said solder connections to have a substantially larger cross section at said component connection pads than at said connection pads at said top surface;

a PCB having a second TCE and having connection pads aligned with said connection pads at said bottom surface, said PCB connection pads being of a larger size than said connection pads at said bottom surface; and

solder connections formed from solder balls between said connection pads at said bottom surface and said PCB connection pads with said larger size pads causing said solder connections to have a substantially greater larger cross section at said PCB connection pads than at said connection pads at said bottom surface; and

wherein connections formed between said component connection pads and said PCB connection pads have an hourglass shape, and act to absorb at least a portion of the stress due to differences between said first TCE and said second TCE.

13. Ball grid array mounted circuit of claim 12 wherein said stress relief substrate comprises a flexible polyimide like material having a thickness in the range of about 2 to 5 mils.

14. Ball grid array mounted circuit of claim 12 wherein said connection pads at said top surface capture a plurality of said conductive vias.

15. Ball grid array mounted circuit of claim 12 wherein said conductive vias have a diameter in the range of 1 to 5 mils and a pitch in the range of 2 to 10 mils.

16. Ball grid array mounted circuit of claim 12 wherein said connection pads at said top surface and said connection pads at said bottom surface have a diameter in the range of about 20 to 30 mils.

17. Ball grid array mounted circuit of claim 12 wherein said electronic component is a ceramic package having a TCE of about 7 ppm/degree C and said PCB has a TCE in the range of about 12-25 ppm/degree C.

18. Ball grid array mounted circuit of claim 12 wherein said conductive vias are uniformly spaced throughout said flexible substrate.

19. Ball grid array mounted circuit of claim 12 wherein said conductive vias are located in said flexible substrate only at said connection pads at said top surface.

20. A method for electrically interconnecting an electronic component to a printed circuit board (PCB) comprising the steps of:

providing an electronic component having an exterior surface having an array of connection pads of a first size;

providing a stress relief substrate having a top surface and a bottom surface, spaced conductive vias extending between said top surface and said bottom surface, connection pads at said top surface with each connection pad capturing a plurality of said vias and connection pads at said bottom surface in registration with said connection pads at said top surface, said connection pads at said top surface and said connection pads at said bottom surface being of a second size wherein said second size is smaller than said first size;

providing first solder balls;

providing second solder balls;

positioning said connection pads at said bottom surface at said first solder balls;

positioning said second solder balls at said connection pads at said top surface;

heating said first and second solder balls to a temperature sufficient to melt said first and second solder balls thereby forming a first assembly with said solder balls adhered to said connection pads;

positioning said first assembly so that said second solder balls are aligned with said connection pads of a first size;

heating said second solder balls to a temperature sufficient to melt said second solder balls and form solder connections with said connection pads of a first size shaping said solder connection to have a substantially larger cross section at said connection pads of a first size than at said connection pads at said top surface, said electronic component and said first assembly forming a second assembly;

providing a PCB having an array of connection pads of a third size; and

connecting said second assembly to said PCB.

21. The method of claim 20 wherein said step of positioning said first solder balls at said connection pads at said bottom surface comprises the steps of:

providing a fixture having an array of spaces for receiving solder balls;

loading said first solder balls into said fixture; and

positioning said stress relief substrate so that said connection pads at said bottom surface align with and abut said first solder balls.

22. The method of claim 20 wherein said step of positioning said second solder balls at said connection pads at said top surface comprises the steps of:

providing a fixture having an array of spaces for receiving solder balls;

positioning said fixture so that said array of spaces align with said connection pads at said top surface; and

loading said second solder balls into said fixture.

23. The method of claim 20 wherein said third size is larger than said second size and said step of connecting said second assembly to said PCB comprises the steps of:

positioning said second assembly with said second solder balls aligned with said connection pads of a third size; and

heating said second solder balls to a temperature sufficient to melt said second solder balls and form solder connections with said connection pads of a third size shaping said solder connection to have a substantially larger cross section at said connection pads of a third size than at said connection pads at said top surface.

24. An interposer for making first connections to an electronic component having a first thermal coefficient of expansion (TCE) and second connections to a printed circuit board (PCB) having a second TCE in a ball grid array mounted circuit comprising:

a stress relief substrate having a top surface and a bottom surface;

spaced conductive vias extending between the top surface and said bottom surface;

connection pads at said top surface with each connection pad capturing at least one of said vias;

said first connections formed from solder balls between said connection pads at said top surface and connection pads located at a surface of said electronic component wherein said first solder connections have a substantially smaller cross sectional area at said connection pads at said top surface than at said connection pads located at said electronic component;

connection pads at said bottom surface in registration with said connection pads at said top surface;

said second connections formed from solder balls between said connection pads at said bottom surface and connection pads located at said PCB wherein said second solder connections have a substantially smaller cross sectional area at said connection pads at said bottom surface than at said connection pads located at said PCB; and

wherein a combination of said first connections and said second connections have hour-glass shapes which are sufficiently compliant to absorb at least a portion of stress related to a difference in said first TCE and said second TCE.

25. The interposer of claim 24 wherein said stress relief substrate comprises a flexible polyimide-like material having a thickness in the range of about 2 to 5 mils.

26. The interposer of claim 25 wherein said conductive vias have a diameter in the range of 1 to 5 mils and a pitch in the range of 2 to 10 mils.

27. The interposer of claim 26 wherein said connection pads at said top surface and said connection pads at said bottom surface have a diameter in the range of about 20 to 30 mils.